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The dawn of Ga_2O_3 HEMTs for high power electronics - *A review*

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ABSTRACT

Recently, there is a growing interest in Gallium Oxide (Ga_2O_3) as a promising semiconductor material for intended applications in RF, power electronics, and sensors with high capabilities over existing technologies due to its excellent material characteristics like large bandgap, well-controlled doping, and availability of large size inexpensive substrates. Bulk crystals of monoclinic β-Ga_2O_3 can be grown using melt growth techniques, which ensures large, uniform substrates with relatively low-cost per wafer as compared to GaN and SiC substrates which are usually grown using vapor growth techniques. A large critical field of β-Ga_2O_3 is beneficial for improving the DC performance of high voltage rectifiers and metal oxide semiconductor field-effect transistors (MOSFETs) and facilitates further lateral scaling of FETs for improved RF performance. Band structure of β-Ga_2O_3 indicates difficulty in p-type conductivity, so previously reported most of the β-Ga_2O_3 MOSFETs have been depletion mode, although enhancement mode operations were also demonstrated using recess-gate and charge-trapping gate stack structure. The β-Ga_2O_3 heterostructures have been widely reported using a high-quality epitaxial layer of β-$(Al_xGa_{1-x})_2O_3$ after alloying Al with Ga_2O_3. The β-Ga_2O_3 modulation-doped FETs (MODFETs) have shown two-dimensional electron gas (2DEG) density of $\sim 10^{12}$ cm^{-2} that form a good quality channel at the interface. Despite low room temperature electron mobility of around 180 $cm^2\ V^{-1}s^{-1}$, peak mobility of around 2800 $cm^2\ V^{-1}s^{-1}$ at 50 K was measured in the latest reported experimental work of β-Ga_2O_3 MODFET. III-nitride based GaN high electron mobility transistors (HEMTs) have been widely used in high power electronics and have shown 2DEG density $\sim 10^{13}$ cm^{-2} and channel mobility of 2000 $cm^2\ V^{-1}s^{-1}$. This paper gives a perspective of Ga_2O_3 material towards making high electron mobility transistors (HEMTs) for a certain class of RF applications. Due to low in-plane lattice mismatch, a high-quality epitaxial layer of GaN and AlN have been grown on β-Ga_2O_3. Furthermore, due to the inherent polarization property of III-nitrides and large bandgap, higher 2DEG density $\sim 10^{13}$ cm^{-2} and large conduction band offset >1.5 eV can be expected in AlN/β-Ga_2O_3 heterostructure. The various defects in WBG devices and their effects on the reliability aspects are also addressed.

1. Introduction

Now-a-days the β-Ga_2O_3 is one of the potential materials of choice of worldwide researchers due to its suitable material properties for high power electronics. It occurs in five different phases such as α, β, γ, δ and ε. Out of these, the monoclinic β-Ga_2O_3 is most stable and technologically relevant [1]. The crystal structure of β-Ga_2O_3 has a center of symmetry but lacks any special properties like polarity, piezoelectricity, ferroelectricity, etc. [2]. β-Ga_2O_3 has an ultra-wide bandgap (E_g) of 4.4–4.9 eV [3–5], making it suitable for applications as deep UV TCO (transparent conducting oxide) and buffer layer for HEMT application. The n-type Ga_2O_3 is easily available using impurities like Si, Ge, Sn, F, and Cl as shallow donors with tunable conductivity from 10^{-12} to 10^2 S cm^{-1} [6–12], also evidence of p-type conduction in undoped β-Ga_2O_3 have been demonstrated, by identifying gallium (Ga) vacancy as a possible acceptor impurity with an energy level of 1.1 eV above the valence band edge (E_V) [13]. On the contrary, Kyrtsos *et. al.* [14], reported the absence of p-type conductivity in Ga_2O_3 due to deep acceptor levels of dopants. Nevertheless, to date growing p-type β-Ga_2O_3 is still in infant stage, its full-scale realization will open new dimensions for β-Ga_2O_3 applications.

In the current scenario, WBG (Wide Band Gap) semiconductor materials such as SiC (Silicon Carbide) and GaN (Gallium Nitride) are dominating in high power electronics applications. However, material

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limit of GaN puts an ultimate cap on high breakdown fields—a key requisite for high power devices. On the other hand, continued interest from potential development agencies and successful defense applications, Ga_2O_3 is going to be critical for further material research, growth and device technology. The β-Ga_2O_3 band structure and material properties are discussed in Section 2, followed by chronological development of β-Ga_2O_3 based devices such as Schottky diodes and FETs—MESFETs, MOSFETs, and MODFETs in Section 3. The modulation-doped β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ heterostructures, calculation of 2DEG density, 2DEG channel mobility and breakdown voltage are discussed in Section 4 followed by polarization effects in III-Nitrides and β-Ga_2O_3 material in Section 5. Section 6 includes self-heating and thermal management of β-Ga_2O_3 devices followed by a comprehensive discussion on reliability issues of WBG devices in section 7. Finally, the conclusions are drawn in Section 8.

2. Crystal structure and material properties of β-Ga_2O_3

He et al. [5], reported the electronic structure and thermodynamic properties of the β-Ga_2O_3 using density functional theory (DFT). Fig. 1 shows the electronic band structure of β-Ga_2O_3, with almost flat valence band maxima and conduction band minima at the zone center. The extracted value of energy band gap, E_g of 4.69 eV (direct) and 4.66 eV (indirect) finds good agreement with values obtained using other measurements: optical absorption [3,4]. The effective mass of electron, m_e^* in a semiconductor largely affects transport property of the semiconductor material. For β-Ga_2O_3 material it was calculated as 0.342 m_o, (where m_o is free electron mass), but rather more flat valence band led large effective mass of holes and diminished hole mobility [5]. Actually, holes form localized polarons, *i.e.* self-trapped holes [15] and are not free to move. The β-Ga_2O_3 crystal structure with lattice parameters (a = 12.2 Å, b = 3.0 Å, c = 5.8 Å) is shown in Fig. 2 [16]. Each unit cell consists of two crystallographically non-equivalent Ga positions with tetrahedral (Ga I) and octahedral (Ga II) geometry. Oxygen atoms occupy three different crystallographically different locations—O (I), O (II), and O (III) and are arranged in distorted cubic array coordinated triangularly (two atoms) and tetrahedral (one atom). Due to different positioning of gallium and oxygen atoms, Ga_2O_3 shows anisotropic optical, electrical and physical properties such as highest thermal conductivity of 0.27 W $cm^{-1}K^{-1}$ in (010) plane, a value almost three times as of in (100) plane [17,18].

Also, it is worth noting that bulk β-Ga_2O_3 (010) oriented crystals grown by EFG method can be cut along $(\bar{2}01)$ plane. Subsequently, this has rendered possible potential application such as growing III-nitrides (GaN, AlN, and InN) on $(\bar{2}01)$ β-Ga_2O_3. Further this can facilitate

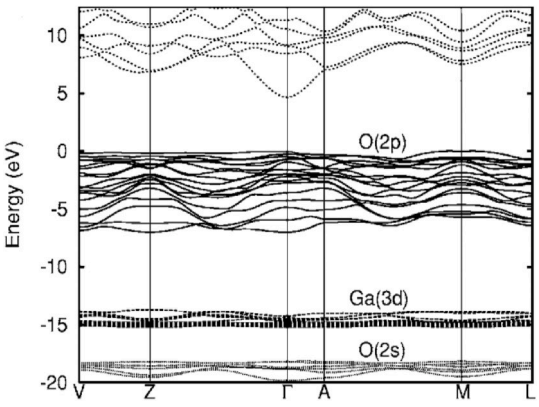

Fig. 1. β-Ga_2O_3 band structure at zero pressure, Fermi level aligned to zero. Uppermost valence band formed by O(2p) states with width of 7 eV, Conduction band minima at Γ (direct band gap 4.69 eV) and at M-Γ indirect band gap 4.66 eV, figure adapted from Refs. [5].

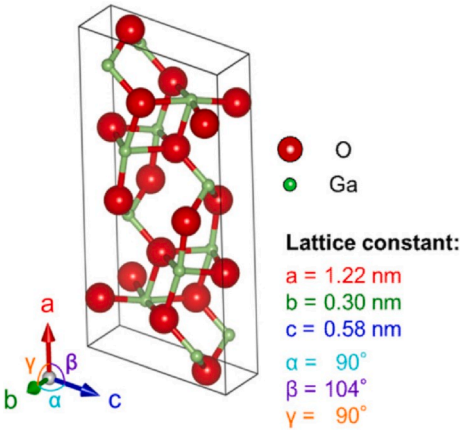

Fig. 2. Unit cell of β-Ga_2O_3 crystal, figure adopted from Ref. [16].

realization of AlN/β-Ga_2O_3 heterostructure as lattice mismatch between $(\bar{2}01)$ β-Ga_2O_3 and (0002) AlN was reported as 2.4% and conduction band offset (CBO) equal to 1.75 eV at the heterointerface [19].

Due to its large E_g, a higher breakdown electric field (E_{BR}) in the order of 8 MV cm^{-1} [20] and high breakdown voltage (V_{BR}) can be achieved. Currently β-Ga_2O_3 single bulk crystal of superior quality with large diameter ranging from 1 inch to 4 inch [21–25] as shown in Fig. 3 have been grown using well-known various melt-growth techniques: Czochralski [21,22], floating zone [23,24], and edge-defined film-fed growth (EFG) [24,25] as shown in Fig. 4, and vertical Bridgeman methods [26].

2.1. β-Ga_2O_3 material edge in power devices

Low-cost β-Ga_2O_3 substrate and growth of high quality (controlled thickness and doping) epitaxial film provides β-Ga_2O_3 an edge over GaN material technology which is suffering from lack of affordable native substrates [27]. Though poor thermal conductivity of monoclinic β-Ga_2O_3 (~0.27 $Wcm^{-1}K^{-1}$) [17] adversely affects high temperature device performance. Also, electron Hall mobility of bulk-doped β-Ga_2O_3 is quite low, < 200 cm^2 V^{-1} s^{-1} [28] at room temperature, due to dominant polar optical (PO) phonon scattering for doping densities ~10^{18} cm^{-3}. On the other hand, at an electric field of 200 kV cm^{-1} average peak electron velocity of around 2 × 10^7 cm s^{-1} [29] is estimated. This value is almost equal to GaN material v_{sat} = 2.0–2.5 × 10^7 cm s^{-1} [30] but electron mobility is one order low over GaN HEMT mobility ~2000 cm^2 V^{-1} s^{-1} [31]. This can be attributed to high electron effective mass in β-Ga_2O_3 material is ~0.25m_0 [28] — approximately 25% more than that in GaN (0.2m_0) [28], and about half value of optical phonon energy, E_{op} (45 meV for β-Ga_2O_3, 90 meV for GaN) [28] which limit the maximum achievable current density in β-Ga_2O_3 devices. Furthermore, low thermal conductivity led increased channel temperature further degrades the mobility of carriers.

Although, due to high values of saturation velocity (2.0 × 10^7 cm s^{-1}) and high E_{BR}, β-Ga_2O_3 HEMTs can largely outperform GaN HEMTs, as indicated by Johnson Figure of Merit (JFOM) —a critical FOM for RF power devices. A high breakdown electric field E_{BR} = 8 MV cm^{-1} [20] for β-Ga_2O_3 is the most promising characteristic for its application in power devices, as BFOM is linearly related to the mobility (μ), whereas strongly (cube) corresponds with E_{BR}. This FOM for Gallium Oxide material is much higher than other WBG semiconductor materials as shown in Table 1, other semiconductor materials—Si, SiC, and GaN are also included for comparison. These values are good indications for evaluation of β-Ga_2O_3 material for possible high power applications. Fig. 5 [20] shows the maximum electric field of WBG semiconductors.

Fig. 6 [32] shows estimated pf^2 characteristics ($V_{BR} f_T \leq E_{MAX} v_{eff}/\pi$) i.e. JFOM for comparing β-Ga_2O_3 and GaN HEMTs on their RF

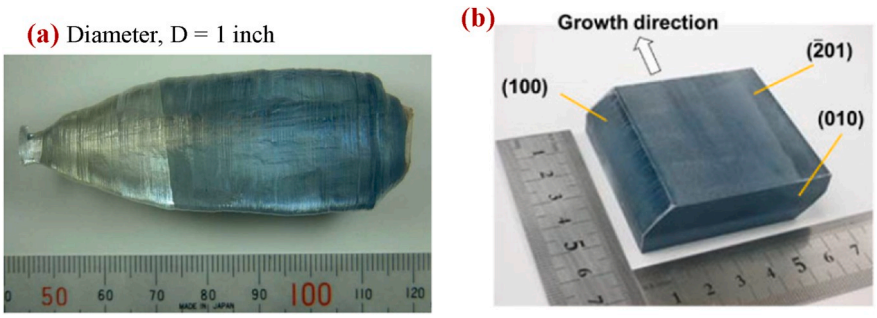

Fig. 3. β-Ga_2O_3 bulk crystals grown using **(a)** floating zone, crystal grown along (100) direction, From Refs. [22], **(b)** EFG, hexagonal prism of size 55 × 60 × 18 mm cut perpendicular to (010) direction, figures adopted from Refs. [23].

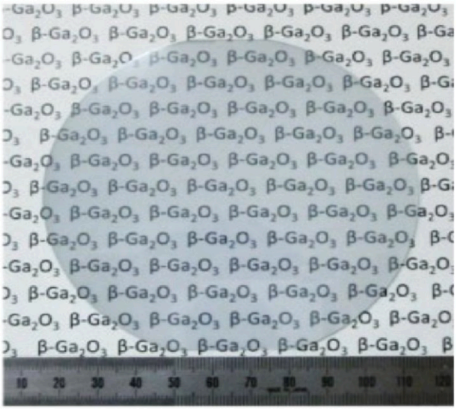

Fig. 4. β-Ga_2O_3 substrate of 4 inch diameter made from bulk crystal of size 110 × 110 × 6 mm, with surface orientation $(\bar{2}01)$ grown using EFG process, figure adopted from Ref. [23].

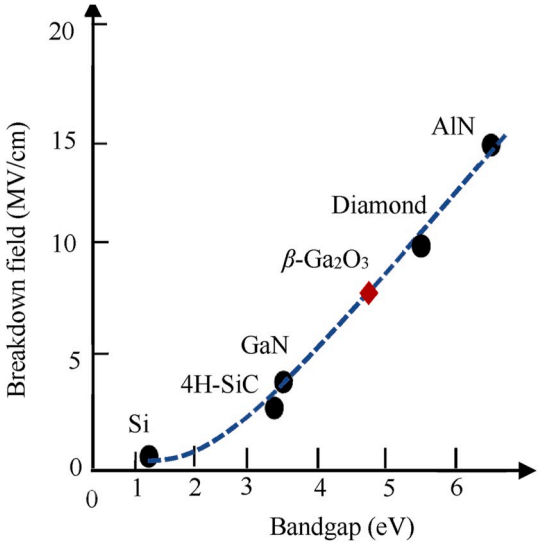

Fig. 5. Electric breakdown fields corresponding to bandgap of major WBG semiconductor material, figure redrawn from Ref. [20].

Table 1
Major properties of WBG semiconductor materials and different FOMs for RF performance evaluation.

Parameters	Si	4H–SiC	GaN	β-Ga_2O_3
Energy band gap, E_g (eV)	1.1	3.2–3.3	3.4	4.5–4.9
Intrinsic carrier concentration, n_i (cm^{-3})	10^{10}	10^{-9}	10^{-10}	10^{-24}
Electric breakdown field, E_{BR} (MV cm^{-1})	0.3	3.0	3.3	8.0
Relative dielectric constant, ε_r	11.8	10	9.0	10
Electron mobility, μ_n ($cm^2\ V^{-1}\ s^{-1}$)	1350	700	2000 (2DEG) [31]	200 [28]
Saturation velocity, v_{sat} (10^7 cm s^{-1})	1.0	2.0	2.0–2.5 [30]	2.0 [29]
Thermal conductivity, k (W $cm^{-1}\ K^{-1}$)	1.5	3.3–4.5	1.3	0.27(010) [17]
$JFOM_{Si}$, ($v_{sat}\ E_{MAX}/2\pi$)	1.0	20	27.5	40
$BFOM_{Si}$ ($\mu_n\ \varepsilon_r\ E^3_{MAX}$)	1.0	439	1503	2380
$BHFFOM_{Si}$ ($\mu_n\ E^2_{MAX}$)	1.0	51.8	179.2	105

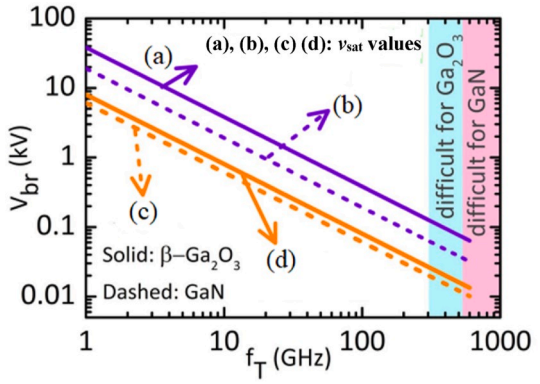

Fig. 6. Maximum operating voltage versus cut-off frequency for β-Ga_2O_3 and GaN HEMT. For β-Ga_2O_3 v_{sat} of 1.5 × 10^7 (a) and 3.15 × 10^6 cm s^{-1} (d), E_{MAX} of 8 MV cm^{-1}, and for GaN v_{sat} of 2.0 × 10^7 (b) and 6.3 × 10^6 cm s^{-1} (c), E_{MAX} of 3 MV cm^{-1} were used. In both curves (violet and orange) β-Ga_2O_3 outperforms GaN HEMT, although it is only marginal in lower curve, figure redrawn from Ref. [32]. (For interpretation of the references to color in this figure legend, the reader is referred to the Web version of this article.)

performances. Recently in $(Al_{0.4}Ga_{0.6})O_2/Ga_2O_3$ modulation doped FET the low temperature electron velocity of ~1.1 × 10^7 cm s^{-1} [33] was measured. It is also estimated that β-Ga_2O_3 based HEMTs can give reasonable high RF output power over GaN HEMTs in low frequency region (up to 10 GHz, X band), but would require more wider periphery to match GaN HEMT DC performances [32].

3. β-Ga_2O_3 based FETs and its performances

Higashiwaki et al. [20] demonstrated the first Ga_2O_3 metal-semiconductor field effect transistor (MESFET) by growing Sn-doped homo-epitaxial layer of Ga_2O_3 on Mg-doped β-Ga_2O_3 (010) single-crystal substrate. This Ga_2O_3 FET showed maximum drain current of 15 mA, and transconductance (g_m) of 1.5 mS at V_{DS} = 40 V and V_{GS} = 2 V. Although device electrical performance was limited by high

source/drain (S/D) contact resistance, and significant leakage current through un-passivated Ga_2O_3 epitaxial layer led small I_{ON}/I_{OFF} ratio of ~10^4. Device schematic and input/output characteristics are shown in Fig. 7 (a) [33].

Subsequently, Higashiwaki et al. [34] developed depletion-mode (D-mode) Ga_2O_3 metal oxide semiconductor FETs (MOSFETs) by adopting Si-ion (n^{++}) doping in S/D access regions for improved Ohmic contacts, as shown in Fig. 7 (b) [34]. Aluminum oxide (Al_2O_3) was used as a gate dielectric and for surface passivation to put a check on leakage currents. The D-MOSFET showed improved electrical performance over Ga_2O_3 MESFET and achieved maximum drain current density (I_{DMAX}) of 39 mA mm^{-1} at $V_{DS} = 20$ V, $V_{GS} = 4$ V, large I_{ON}/I_{OFF} ratio of ~10^{10}, low leakage current in the order of pA/mm, and wide range of operating temperature. The poor thermal conductivity of Ga_2O_3 devices leads to self-heating effect which is dominant at higher drain bias and results in negative output conductance. It is worth noting that this high n^{++} doping of ~10^{19} cm^{-3} in S/D access regions has set a precedent for most Ga_2O_3 power devices to minimize S/D access resistances. Further efforts led by technological developments helped to realize delta doping in the channel regions. This silicon (Si) (n-type dopants) delta doping in β-Ga_2O_3 epitaxial layer aided channel mobility and high charge density. Simultaneously, multiple delta doping was also used in S/D access regions to achieve low contact resistance.

Krishnamoorthy et al. [35] demonstrated delta-doped β-Ga_2O_3 FET using unintentionally doped (UID) β-Ga_2O_3 epitaxial layers comprising of Si delta-doped layers on Fe-doped semi-insulating (SI) (010) β-Ga_2O_3 substrate. A sheet charge density of ~10^{13} cm^{-2}, and Hall electron mobility of ~34 cm^2 $V^{-1}s^{-1}$ were measured in gate recess delta-doped device structure as shown in Fig. 7 (c) [35], shows I_{DMAX} of 236 mA mm^{-1}, and g_m of 26 mS mm^{-1}. Subsequently, other promising n-type dopants like Sn, and Ge were explored for improved power performance, and a maximum electric field of 3.8 MV cm^{-1} [36] for gate-drain spacing (L_{GD}) of 0.6 μm, and higher carrier mobility of ~111 cm^2 $V^{-1}s^{-1}$ [37] were reported. β-Ga_2O_3 on insulator field-effect transistor (GOOIFET) [38,39] demonstrated depletion-mode (D-mode) as well as enhancement-mode (E-mode) operation through surface depletion and achieved record high I_{DMAX} of 1.5 Amm^{-1} [39] using highly doped nano-membrane channel. High-voltage vertical Ga_2O_3 FETs achieved breakdown voltage, $V_{BR} > 1$ kV [40] and substantially increased using field-plate topology [41–43] which showed $V_{BR} > 2.32$ kV [43]. To date, the β-Ga_2O_3 MOSFETs are dominated by D-mode devices. However, the E-mode operation of the power devices ensures protected functionality and receding off-state power dissipation. E-mode operation of β-Ga_2O_3 FETs [44–48] was realized using wrap-gate fins [44], mechanically exfoliate thin films and hafnium oxide (HfO_2) as gate dielectric [45], undoped channel [46], and partial removal/depletion of active channel through gate-recess [47,48]. As gate-recess reduces channel mobility, a major breakthrough to achieve E-mode operation is reported recently by Feng et al. [49] using ferroelectric charge storage gate stack.

As discussed before, E_{MAX} of 3.8 MV cm^{-1} [36] for β-Ga_2O_3 MOSFET was experimentally verified. This high value of E_{MAX} led to the significant scaling of the lateral device. This has enabled potential power-switching applications and improved RF performance as indicated by BFOM and JFOM, respectively. The β-Ga_2O_3 devices with excellent RF performance were reported [50–53]. First, RF performance of β-Ga_2O_3 MOSFETs has been demonstrated by Green et al. [50]. The 'T' gate length ($L_G = 0.7$ μm) in this device has a highly doped (10^{19} cm^{-3}) cap layer to minimize contact resistance. The MOSFET achieved current gain cut-off frequency (f_T) of 3.3 GHz, and maximum oscillation frequency (f_{MAX}) of 12.9 GHz. Subsequently, f_T of 5.1 GHz, and f_{MAX} of 17.1 GHz on β-Ga_2O_3 MOSFET with 'T' gate $L_G = 0.14$ μm and 65 nm thin Si-doped channel were reported by Chabak et al. [51]. Large signal RF measurement using pulse-mode operation to avoid self-heating in field-plated β-Ga_2O_3 MOSFETs as shown in Fig. 8 (a) was reported by Singh et al. [52]. The record power added efficiency (PAE) is 12% while CW large signal PAE is approximately 9%. Recently, Xia et al. [53] have reported delta-doped β-Ga_2O_3 MESFET as shown in Fig. 8 (b), with further device scaling ($L_G = 0.12$ μm, 20 nm thin channel), and highly doped (10^{20} cm^{-3}) S/D cap regions. The MESFETs achieved an extrinsic f_T of 27 GHz, I_{DMAX} of 260 mA mm^{-1}, and g_m of 44 mS mm^{-1}, which can be further explored toward potential millimeter wave applications.

3.1. *β-Ga₂O₃ power rectifiers*

WBG based Schottky rectifiers deliver fast switching speed, which helps to achieve high efficiency of induction motor controllers and power supplies [54]. Also, these power Schottky diodes show various advantages. Compared to conventional Si rectifiers, they have very high ~10 times larger E_{MAX} and very low ~400 times lower on-resistance (R_{ON}) [55–57]. Various Ga_2O_3 based rectifiers [58–62] have been

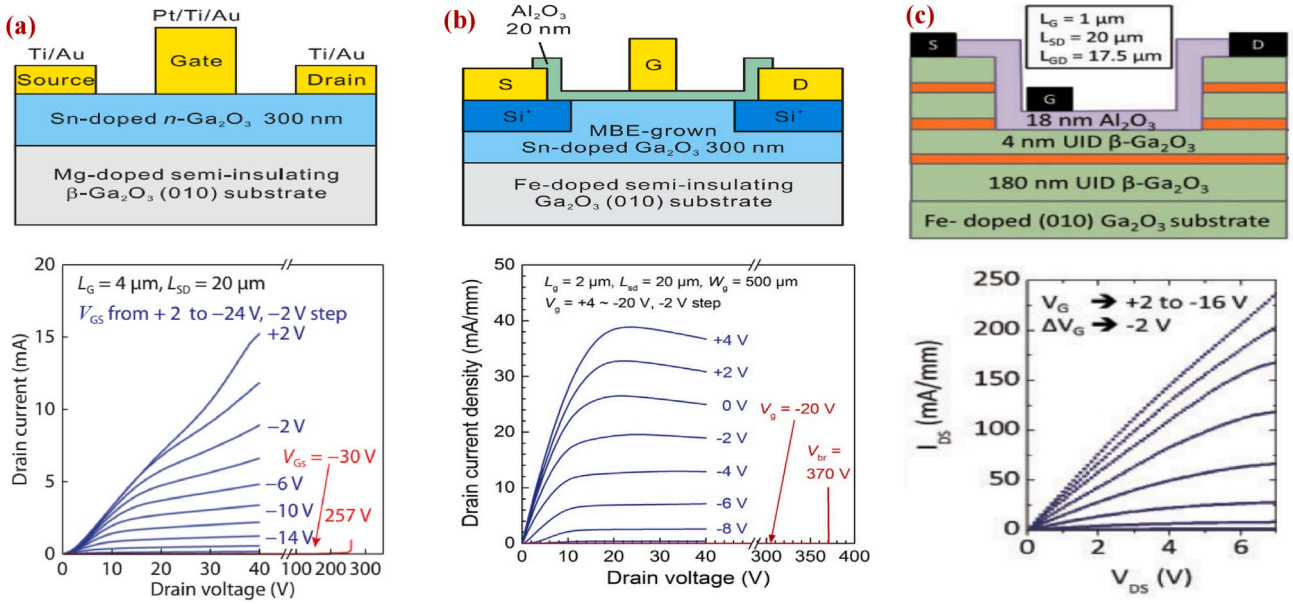

Fig. 7. Schematic cross sections and output characteristics of **(a)** Sn-doped β-Ga_2O_3 FET, figures adopted from Ref. [20], **(b)** Highly doped S/D regions in β-Ga_2O_3 D-mode MOSFET, figures adopted from Ref. [34], **(c)** delta-doped β-Ga_2O_3 FET, figures adopted from Refs. [35].

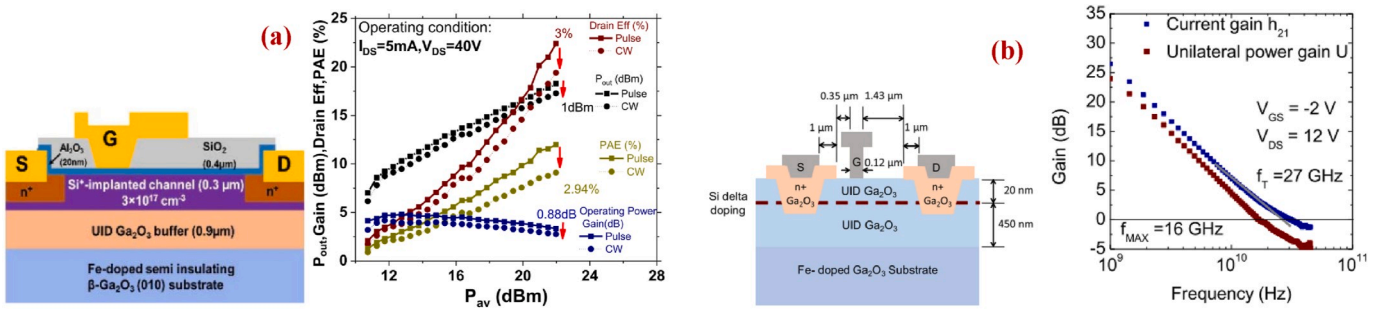

Fig. 8. Schematic cross sections and **(a)** Large signal CW and pulsed measurements at 1 GHz of field-plated Ga_2O_3 MOSFET, pulse measurement led reduced self-heating resulted in high values of drain efficiency 22.4%, and output power density of 0.13 W mm^{-1}, figures adopted from Refs. [52], **(b)** Small signal performance of delta-doped β-Ga_2O_3 MESFET, low value of ratio $f_{MAX}/f_T \sim 0.6$ was due to high gate and source resistance, figures adopted from Refs. [53].

demonstrated to have a high breakdown voltage (V_{BR}) > 1 kV [60,61], either with or without field-plate for lateral distribution of electric field. The high value of BFOM (V_{BR}^2/R_{ON}) ~154 MW cm^{-2} was achieved for a 105 μm diameter diode [61]. Although, Ga_2O_3 rectifiers are affected by the presence of defects and breakdown in the depletion region near the electrodes [58–62], it should be highlighted that to realize P-i-N for Ga_2O_3 rectifier technology is almost impossible [63] because p-type doping are not yet demonstrated. Thus, low turn-on and ultra-high breakdown voltages can't be achieved simultaneously.

In summary, experimental results have established promising DC and RF performance of these β-Ga_2O_3 based FETs, MOSFETs, MESFETs, and Schottky barrier diodes.

4. Modulation-doped β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ heterostructures

Early efforts to realize β-Ga_2O_3 heterostructures have faced challenges in relation with Ga_2O_3 solubility and surface roughness induced between binary and ternary Ga_2O_3 materials [64]. Furthermore, carrier confinement at the heterostructure was far-fetched, but very early development was made to alloy Al with Ga_2O_3 for possible β-$(Al_xGa_{1-x})_2O_3$ (AGO) [65]. Oshima et al. laid down the possibility of β-$(AlGa)_2O_3/Ga_2O_3$ HEMTs by growing β-$(AlGa)_2O_3$ thin films on a (010) β-Ga_2O_3 substrate using plasma-assisted MBE (PA-MBE) [66]. The Al content up to 61% maintained β-phase of grown AGO films. Subsequently, AGO films were grown on sapphire substrates by pulsed laser deposition (PLD), resulted in tunable bandgap of $(AlGa)_2O_3$ films as 5.34 eV, and 5.74 eV with Al content of 0.22 and 0.53, respectively [67]. First, β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ (AGO/GO) heterostructure was reported by Kaun et al. [68] and post growth investigations revealed that undoped AGO layer and interface abruptness prevent carrier confinement at the interface.

The next important developments towards modulation-doped FETs (MODFETs) or heterojunction FETs (HFETs) related to the fabrication of MODFETs and validation of carrier confinement at the heterointerface. Wong et al. [69] reported about accumulation of Si contamination on a Ga_2O_3 substrate during melt growth. It is used as unintentional dopants in the AGO epitaxial layer which enabled modulation-doping in the AGO/GO heterostructure, and the sheet charge density of ~3 × 10^{12} cm^{-2} was recorded at the heterojunction [70]. On the other hand, Ahmadi et al. [71] used Ge as a dopant to AGO barrier layer to fabricate AGO/GO MODFETs. The group also demonstrated the positive effect of Ga-polishing prior to growth on surface morphology and reduction of contaminants (Si and Ge) at the interface. Further, Krishnamoorthy et al. [72] used Si- delta doping in AGO layer to realize modulation-doped β-$(Al_{0.2}Ga_{0.8})_2O_3/Ga_2O_3$ FET. 2DEG sheet charge density (n_s) of 5 × 10^{12} cm^{-2} and Hall mobility of 74 cm^2 V^{-1}s^{-1} were measured. First, a time spacer layer was introduced between AGO barrier and GO buffer layers for improved charge modulation in AGO/GO MODFETs [72]. The major developments of AGO/GO MODFETs are shown in Fig. 9.

The DC performance of developed AGO/GO MODFETs so far has been affected by high contact resistance and parasitic channel in the buffer layer due to various contaminants at the heterointerface. These issues were efficiently addressed by Zhang et al. [73]. The high mobility and quantum transport in modulation-doped AGO/GO heterostructures have been achieved. The two samples were grown on Fe-doped (010) β-Ga_2O_3 using PA-MBE, consisting of an UID β-Ga_2O_3 buffer layer (130 nm/360 nm), 27 nm AGO barrier layer with Al composition of 0.18, and Si delta doped layer of donor concentration 4.7 × 10^{12} cm^{-2}. Source/-drain access regions were highly doped with Si (>10^{20} cm^{-3}). The yielded contact resistance is of 4.1 Ω mm for samples with a 360 nm buffer layer. The room temperature mobility is 180 cm^2 V^{-1}s^{-1} while very high low temperature carrier mobility is as high as 2790 cm^2 V^{-1}s^{-1} at 50 K and estimated n_s = 1.5 × 10^{12} cm^{-2}. Low density of diffused impurity in a sample with thicker buffer layer (>360 nm) is attributed to a significant increase in mobility at low temperature. But the same mobility values (162/180 cm^2 V^{-1}s^{-1}) recorded at room temperature from these samples with different buffer layers are attributed to strong polar optical phonon scattering [28]. Fig. 10 shows device schematic of AGO/GO MODFET [72,73]. The 2DEG AGO/GO MODFET using double heterostructures shows an increase to 3.85 × 10^{12} cm^{-2} in charge density and the high value of I_{DMAX} of 257 mAmm^{-1} [74] was measured. Recently, Okumura et al. [75] reported AGO/GO MODFET and AGO channel MESFET using Sn-doped β-$(Al_XGa_{1-X})_2O_3$ layers with Al composition of 0.08 and 0.16 respectively on Fe-doped semi--insulating (010) β-Ga_2O_3 substrate.

In summary, either intentional dopants (Si/Ge/Sn) or delta doping in most AGO barrier of modulation-doped β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ heterostructures, it is also observed that accumulated impurities on β-Ga_2O_3 substrate enabled parallel channel in buffer layer, adversely affected the device electrical performance. Also auto-doping of these impurities cannot be utilized for complex design structures due to the lack of control on dopant concentration or doping profile [71]. Typical values of n_s are estimated in the order of ~10^{12} cm^{-2} with donor concentration of ~10^{12} cm^{-2} in the delta layer. The other important parameters affecting n_s are CBO (0.4–0.6 eV) at the interface, Al mole fraction (up to 20%) in the AGO barrier, and buffer layer thickness. Different key parameters reported for a couple of β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ heterostructures [72,73] are plotted and compared in Fig. 11. This is an effort to highlight the improved device performance by using high doping in S/D access regions for low contact resistance and thicker buffer layer for reduced background impurities.

The three important parameters such as 2DEG charge density, channel mobility, and blocking voltage of β-$(Al_XGa_{1-X})_2O_3/Ga_2O_3$ heterostructure based MODFETs are discussed as follows.

4.1. 2DEG density

It is observed that AGO barrier layer in MODFETs accumulated Si (peak concentration of 10^{19} cm^{-3}) as unintentional dopant on β-Ga_2O_3 substrate, achieve 2DEG carrier density of 3 × 10^{12} cm^{-2} [70], but they

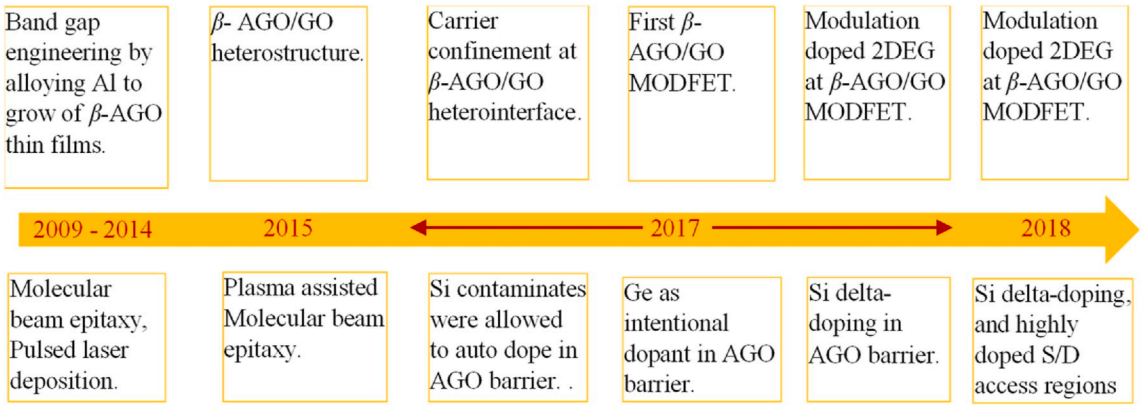

Fig. 9. Major developments of β-$(Al_XGa_{1-X})_2O_3/Ga_2O_3$ MODFETs, highlighting AGO/GO heterostructure, carrier confinement, and modulation-doping.

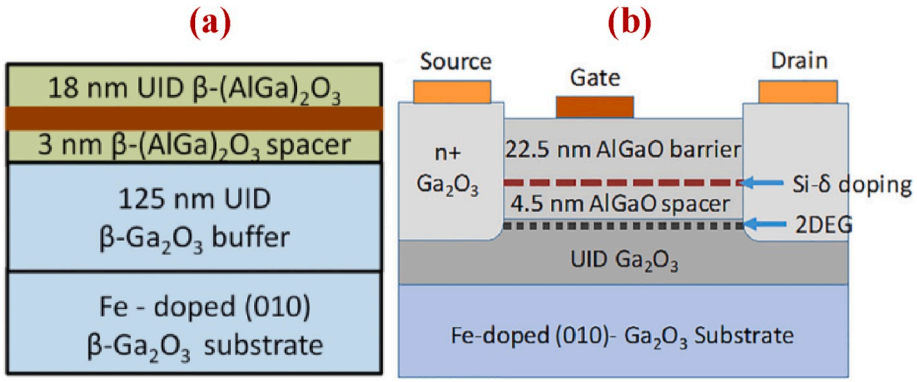

Fig. 10. Schematic epitaxial layers of Si delta-doped β-(AGO)/GO heterostructures **(a)** due to high contact resistance, MODFET characteristics are measured on wide S/D contact access regions (100 μm) [72], **(b)** MODFET structure having AGO barrier of thickness 27 nm and buffer layer of 360 nm, highly doped S/D contact regions are used to achieve ohmic contacts with contact resistance as low as 4.9 Ω mm [73], figures adopted from Refs. [72].

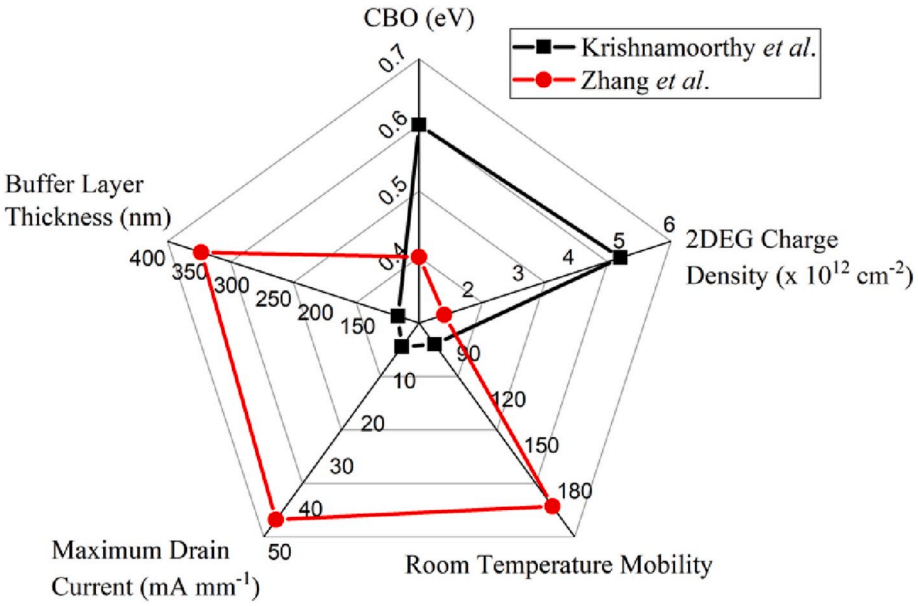

Fig. 11. Spider chart of key parameters reported in Ref. [72], and [73]. It may be concluded that overestimation of 2DEG density by assuming higher CBO values does not reflect in improved device performance.

suffer from electronically detrimental parallel conduction. This auto-doping also lacks control on dopant concentration or doping profile, and hence cannot be utilized for complex design structures [71]. A moderate Si delta-type- [72,73] or Ge/Sn- [71,75] intentional doping ($\sim 10^{12}$ cm^{-2}) in the barrier layer, relatively thick buffer layer [73], and Ga-polishing [71] prior to barrier layer growth can improve device

performance in absence of parallel conduction in the barrier layer.

Although the suppression of Si contaminants lead to reduced 2DEG carrier density, but higher values of I_{DS} of 257 mA mm^{-1} [73], and g_m of 39 mS mm^{-1} [73,74], probably due to elimination of parallel channel. High Al concentration in the β-$(Al_xGa_{1-x})_2O_3$ barrier layer produces higher CBO at the interface, which results in higher 2DEG carrier density [68]. However, generally, Al mole fraction $x \leq 0.2$, thermally stable Al_2O_3 limits solubility in β-Ga_2O_3 [68]. Lower CBO at the heterointerface could be also one of the reasons for the formation of parasitic channel in the barrier layer due to poor confinement of charge carriers. Thus, band offsets at the β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ interface seem inevitable to quantify more accurate 2DEG density. The issue was addressed by Wakabayashi et al. [76]. Band alignments were investigated using electron and X-ray photoemission spectroscopy (XPS). The band alignment of β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ was found as type-I, where the CBO value of 0.52 ± 0.08 eV for $x = 0.37$ and and 0.37 ± 0.08 eV for $x = 0.27$, respectively. It is also noted that higher 2DEG density is resulted by considered large CBO (0.6 eV) in the previously discussed Si delta-doped MODFET [72]. On the other hand, thinner spacer layer (a few nm), which provides spatial separation between ionized donors and modulation-doped 2DEG channel, may also lead to enhanced carrier density in the channel but sacrificed electron mobility due to inflated interactions between ionized donors and free carriers.

4.2. 2DEG channel mobility

In HEMTs, high channel mobility gives superior DC switching performance in terms of efficiency and loss. Peak mobility of 2790 cm^2 $V^{-1}s^{-1}$ at 50 K and 180 cm^2 $V^{-1}s^{-1}$ at 300 K [73], appears to be the best among β-Ga_2O_3 based heterostructures. The increase in channel mobility recorded at low temperature in higher thickness of buffer and spacer layer in β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ MODFETs, is due to short diffusion of impurities from substrate surface. Although, at room temperature, mobility values (<200 cm^2 $V^{-1}s^{-1}$) are attributed to dominant phonon scattering (PO) [28].

Furthermore, several reports on analysis of the scattering mechanism of limiting electron mobility [77–80] and carrier transport analysis [81,82] in β-Ga_2O_3 crystal have been reported, helpful to analyze electron mobility for improving device performance. In an anisotropic crystalline structure such as monoclinic β-Ga_2O_3, non-polar phonon scattering is the dominant mechanism [77]. On the other hand, Ma et al. [78] suggested polar phonon scattering is dominant for low-doping densities, and deduced phonon energy of 44 meV from the transport properties. Recently, Zhang et al. [82] have evaluated effects of acoustic phonon (AC) scattering under the frame of deformation potential and relaxation time approximation, and found electron mobility mainly dependent on deformation potential.

4.3. Breakdown voltage

The OFF state of a power switch should sustain a higher field, and for β-Ga_2O_3, it is expected to be as high as 8 MV cm^{-1} [20]. Double heterostructure MODFETs [74] achieve V_{BR} of 428 V, and corresponding E_{BR} of 2.8 $MVcm^{-1}$ without using gate field-plate. The β-Ga_2O_3 MOSFET achieves a high value of V_{BR} and E_{BR} using field-plated topology. The possible integration of field-plate style may help to realize high value of V_{BR}, and E_{BR} for β-Ga_2O_3 based HEMTs.

In summary, the maximum estimated 2DEG density (n_s) of $\sim 5 \times 10^{12}$ cm^{-2} and a low carrier mobility of ~180 cm^2 $V^{-1}s^{-1}$ in β-Ga_2O_3 MODFETs were observed, which are almost one order as below as in AlGaN/GaN HEMT (1×10^{13} cm^{-2}, 1500 cm^2 $V^{-1}s^{-1}$). Although, electron saturation velocity (v_e) of $\sim 2.0 \times 10^7$ cm s^{-1} is the same for both type of technologies, maximum drain current density achievable in these MODFETs/HEMTs is qn_sv_e, where q is electronic charge, n_s is sheet charge density, and v_e is the carrier velocity. Hence, for β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ MODFETs, it is quite a challenge to match with the performance of GaN HEMTs. Nonetheless, higher values of 2DEG density above $\sim 10^{13}$ cm^{-2} and CBO of ~1.5 eV can be realized by possible heterostructure between III-nitride semiconductors (GaN, InN, and AlN) and β-Ga_2O_3, as the former possess high polarization and large band gap. The in-plane lattice mismatch between β-Ga_2O_3 and GaN/AlN was reported as 4.7/2.4% [19,83]. Due to small lattice mismatch between $(\bar{2}01)$ β-Ga_2O_3 on (0002) AlN, $(\bar{2}01)$ β-Ga_2O_3 epitaxial layer could be effectively grown on (0002) AlN [19]. Furthermore, epitaxial growth of AlN on β-Ga_2O_3 using PLD to form heterojunction and investigated band offsets have been reported [19]. The next section describes III-nitride based polarization induced 2DEG sheet charge density in AlN/β-Ga_2O_3 heterojunction based on experimentally reported values of CBO in the AlN/β-Ga_2O_3 heterojunction and by widely used polarization related quantities.

5. Polarizations in III-Nitride and β-Ga_2O_3

Sun et al. [19] reported on $(\bar{2}01)$ β-Ga_2O_3 growth on (0002) AlN/-sapphire templates to form AlN/β-Ga_2O_3 heterojunction. The valence and conduction band offset were measured −0.55 eV and 1.75 eV, respectively, by using high-resolution XPS. Fig. 12 shows a band alignment of AlN/β-Ga_2O_3 [19] heterojunction along with GaN/β-Ga_2O_3 [19,84]. In the current technology of power electronics and HEMTs, III-nitrides and their alloys are key and widely used [85]. Polarization properties of III-nitrides have been widely investigated, and grown AlGaN/GaN heterostructures along Ga- (0001) and N-face $(000\bar{1})$ directions have been demonstrated using metal organic chemical vapor deposition (MOCVD) and plasma-induced MBE (PIMBE) [86–94]. III-nitrides can be grown in wurtzite and zinc blende phases. Due to the inversion asymmetry along the c-axis in the Wurtzite structure, the 0001 and $000\bar{1}$ directions present different surface properties and growth kinetics [85]. The spontaneous polarization (P_{SP}) in III-nitrides are due to lack of inversion symmetry, while piezoelectric polarization (P_{PZ}) is from induced strain between epitaxial films [85–88]. P_{SP} and P_{PZ} in GaN and AlN wurtzite are found to be ten times larger than in conventional III–V and II–VI semiconductor compounds [86]. These high spontaneous polarizations and induced electric fields (E) along the grown epi-direction can produce high interface charge densities (σ). Polarization induced charge density is related as gradient of polarization [86,87], $\sigma = -\nabla P$, where P is the total polarization charge ($P = P_{SP} + P_{PZ}$). Hence, at the interface of two dissimilar material heterostructure,

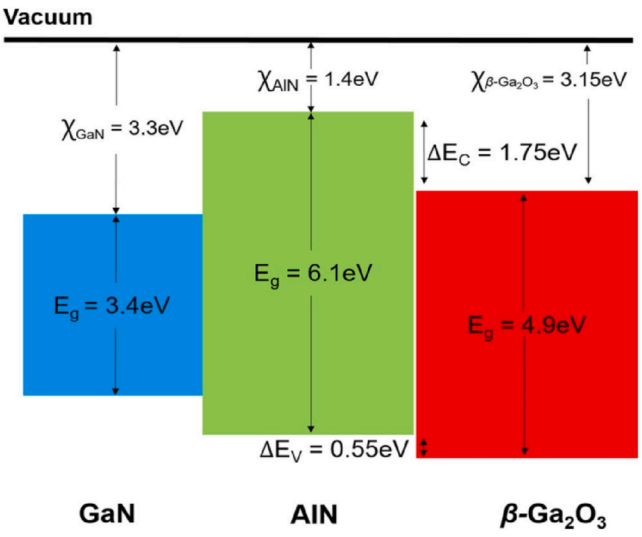

Fig. 12. The band alignment illustration of AlN/β-Ga_2O_3 (type II) and GaN/β-Ga_2O_3 (type I) heterojunction with CBO of −1.75 and 0.55 eV respectively were measured, figure adapted from Ref. [19].

interface charge density can be defined as follows [86,87],

$$\sigma = P_{buffer} - P_{epi} = P_{buffer} - \left(P_{SP,epi} + P_{PZ,epi}\right) \quad (1)$$

where, P_{buffer} and P_{epi} are the total polarization charge of the bottom and top layer of AlN/β-Ga_2O_3 heterojunction. Piezoelectric polarization can be calculated as follows [86,87],

$$P_{PZ} = 2\left(\frac{a_s - a_0}{a_0}\right) e_{31} - \frac{c_{13}}{c_{33}} e_{33} \quad (2)$$

where, a_s as lattice constant of AlN epi-layer, a_0 lattice constant of β-Ga_2O_3, piezoelectric constants: e_{31}, e_{33}, and elastic constants: c_{13}, c_{33}, so the resulted P_{PZ}.

$$P_{PZ} = -0.04692\ C/m^2,\ \textit{So total polarization charge} = P_{SP} + P_{PZ}$$
$$= -0.09 - 0.04692 = -0.136\ C/m^2$$

Total polarization charge of $-0.136\ C/m^2$ translates into 2DEG sheet density of $8.48 \times 10^{13}/cm^2$ at the interface. Table 2 shows values of lattice constants of β-Ga_2O_3, AlN and GaN, spontaneous polarization, piezoelectric and elastic constants of AlN and GaN. It may be concluded that owing to small lattice mismatch (2.4%) and large conduction band offset (1.75 eV), high quality possible AlN/β-Ga_2O_3 heterojunction can achieve high 2DEG density $\sim 10^{13}$ cm^{-2} in more confined band discontinuity at the interface (see Table 3).

6. Self-heating issues and thermal management of Ga_2O_3 devices

β-Ga_2O_3 monoclinic structure has anisotropic and low thermal conductivity values (over other WBG semiconductors, Table 1) which falls in the range of ≈0.10–0.27 W $cm^{-1}K^{-1}$ [17,18] along different crystal axes as discussed earlier in Section 2. Ga and O vacancies in Ga_2O_3 are expected to give rise to unintentional defects and adversely affect thermal and transport properties [11,59,96–98]. Highly anisotropic thermal conductivity of Ga_2O_3 versus temperature is shown in Fig. 13 [17]. Due to poor thermal conductivity, it is expected that Ga_2O_3 devices will suffer from self-heating effect resulting degradation of device performance. Apart from increase in channel temperature and subsequent decrease in electron mobility, a significant drop in cut-off frequency with increasing output power is also expected. Improved RF performance using pulsed signal measurement by reduced self-heating effect in field-plated Ga_2O_3 MOSFET was reported by Singh et al. [52]. Although, looking at the grave of self-heating effects and the importance of thermal management, the merely pulsed operation will not be sufficient and proper thermal management of Ga_2O_3 devices look more crucial for reliable operation at high power. Since heat dissipation is critical in assessing the RF performance of the HEMTs, estimation of thermal resistance (TR) and channel temperature of these devices are proved to be important.

Earlier, a significant reduction in TR was reported by adopting flip-chip (FC) mounting [99–102] the GaN HFETs on highly conductive AlN substrate and epoxy under fill [103] (thermoconductive material is used to fill the air gap between chip and AlN substrate). Taking cue from past approaches developed to alleviate self-heating effects for GaN HEMTs, various solutions have been reported by different researchers

Table 2
Polarization parameters for AlN, GaN, from Ref. [95] and lattice constant of β-Ga_2O_3 from Refs. [16].

Parameters	AlN	GaN	β-Ga_2O_3
Lattice constants (Å)	3.112	3.189	3.04
e_{31} (C/m^2)	−0.53	−0.34	–
e_{33} (C/m^2)	1.5	0.67	–
c_{13} (C/m^2)	127	100	–
c_{33} (C/m^2)	382	392	–
P_{SP} (C/m^2)	−0.09	−0.034	–

Table 3
Deep level traps reported in β-Ga_2O_3 substrate and epitaxial layer; energy level; capture cross section and trap concentration.

Traps Energy Level (eV)	Capture Cross Section (cm^{-2})	Trap Source	Trap Concentration (cm^{-3})	References
E_C – 0.78	7×10^{-15}	Fe-doped substrate ($\bar{2}01$)	1×10^{16}	[98]
E_C – 0.75	5×10^{-14}		1×10^{16}	
E_C – 0.98	(0.1–9) × 10^{-14}	Ge-doped PAMBE on (010) substrate	1.6×10^{15}	[128]
E_C – 0.82	1×10^{-14}	UID Bulk EFG wafer (010)	3.6×10^{16}	[97]

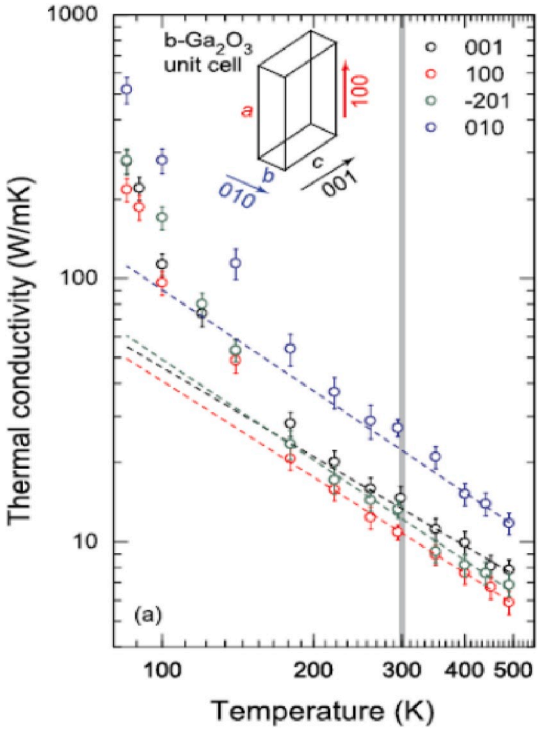

Fig. 13. Thermal conductivity of β-Ga_2O_3 along different crystal directions, figure adopted from Refs. [17].

[104–110] for β-Ga_2O_3 devices. Majority of them include integration of ultra-high thermal conductive diamond as substrate as well as heat-spreader, and various active and passive cooling mechanisms. Low-cost and higher thermal conductive sapphire k = 0.4 W $cm^{-1}K^{-1}$ [111] substrate rather than native Ga_2O_3 substrate was proved to be more effective in mitigating self-heating effects. Zhou et al. [105] demonstrated β-Ga_2O_3 FETs on thermal conductive sapphire substrate instead of Si/SiO_2 insulator substrate, which resulted in low TR (less than 1/3 of that on Si/SiO_2) and higher I_{DMAX} (70% higher that on Si/SiO_2). Using thermal simulation, Oh et al. [106] demonstrated reduced self-heating effects in β-Ga_2O_3 MOSFET on nano-crystalline diamond (NCD) substrate, lowest peak lattice temperature and less degradation of drain current among other substrates like 4H–SiC and β-Ga_2O_3. Cheng et al. [107] examined thermal transport across the Ga_2O_3-diamond interfaces and used time-domain thermoreflectance (TDTR) to measure thermal boundary conductance (TBC) value of 17–1.7/+2.0 MW m^{-2} K^{-1} across van der Waals bonded interfaces. The device structure as shown in Fig. 14 [107] consisted of 500 nm (100) oriented Ga_2O_3 epitaxial layer on different substrates like diamond/-Si/SiC. The simulated device used power density of 10 W mm^{-1} to assess the effect of TBC on the thermal performance of Ga_2O_3 power devices.

Recently, Tadjer et al. [109] showed over 20 times improvement in power density by using highly conductive Cu (k = 3 W $cm^{-1}K^{-1}$ [109]) over Ga_2O_3 substrate to reach target device temperature of 175 °C. The simulated device includes a 1 μm thick Ga_2O_3 epilayer on either Ga_2O_3 (200 μm) or Cu (50 μm) substrates. However, Ga_2O_3 on Cu (50 μm) substrate exhibited ~ 75% reduction in achievable power density from 1 to 12 μm epilayer thickness. Pomeroy et al. [110] measured peak temperature along the β-Ga_2O_3 FET channel using the Raman thermography technique as well as thermal simulations, and demonstrated 75% temperature alleviation by thinning down (010) Ga_2O_3 substrate.

Thermal resistances of Ga_2O_3 and GaN HEMTs on different substrates Ga_2O_3/Sapphire/GaN/SiC were estimated by varying the substrate thickness by Kumar et al. [32]. Both Ga_2O_3 and GaN based devices have a channel thickness of 1 μm, gate length of 250 nm and width of 100 μm were studied, resulting in significantly higher values of TR for Ga_2O_3 HEMT in absence of any substrate over GaN counterparts on GaN and SiC substrates, shown in Fig. 15 [32]. As the channel temperature is equal to 25 °C + TR*1 for net power dissipation of 1 W for the devices with gate width of 0.1 mm, Fig. 15 (b) and **(c)** look quite similar. So for output power of 10 Wmm^{-1}, channel temperature of 284 °C was recorded for 1 μm thick Ga_2O_3 HEMT, as shown by the violet star in Fig. 15 (c). However, to maintain Ga_2O_3 devices junction temperature <200 °C similar to as adopted in GaN HEMTs RF applications [112–114] for safe operations, the maximum RF output power of the Ga_2O_3 (1 μm), and on 350 μm thick sapphire or Ga_2O_3 substrates limited to 7 and 2 W mm^{-1} respectively [32]. Furthermore, an increase in dissipated power from 1 to 7 Wmm^{-1} resulted in 50% drop in cut off frequency due to reduced carrier mobility at elevated temperatures. Additionally, due to lower electron mobility Ga_2O_3 transistors would require larger dimensions over GaN counterparts for similar power rating and it also limits its switching performance [32].

Here, it should be noted that alternate substrates like higher thermal conductive diamond k = 20 W $cm^{-1}K^{-1}$ [115] and low-cost sapphire were widely used to reduce self-heating in β-Ga_2O_3 devices. However, these bottom-side cooling approaches let go of the high quality single crystal Ga_2O_3 native substrate—one of the key motivations of Ga_2O_3 technology. Chatterjee et al. [116] showed an effective approach to thermal management of Ga_2O_3 MOSFETs through flip-chip hetero--integration at the device level (Fig. 16) which helped to keep junction temperature below stipulated value of 200 °C. Subsequently, this design was simulated and achieved improved thermal transient response by ~40% over GaN-on-Si HEMT. The studied Ga_2O_3 MOSFETs were grown on $(\bar{2}01)$ Ga_2O_3 substrate rather than (010) oriented crystals. So, relative thermal improvements are expected to be different due to the anisotropic thermal conductivity of Ga_2O_3. Although, estimated TR values of 94 [116] and 88 mm K W^{-1} [110] were quite similar but significantly higher than 48 mm K W^{-1} [104]. This was attributed to different measurement techniques employed and anisotropic thermal conductivity values of β-Ga_2O_3.

7. Reliability of WBG devices

Since power devices in RF/microwave and power switching electronics operate in tough environmental conditions typically in military and space applications, expected characteristics of these devices are generally at stake, and hence reliability issues concerning known and unknown factors should be accounted while making a final call for specific applications. As compared with WBG materials (diamond, BN, SiC, GaN, Ga_2O_3) silicon technology is more mature and device technology is well understood that led to less reliability issues. Among the WBG materials, SiC and GaN based devices have already made significant progress in power amplifier and/or power switching applications and are expected to serve the demand of new emerging fields like sensors for automatic/self-driving vehicles and motion control system for robotics [54].

Although, the performance of β-Ga_2O_3 devices seems to be promising, many challenges such as growth maturity, thermal management, and material reliability exist, still, it is expected that Ga_2O_3 may supplement more mature SiC and GaN power device technologies [117]. Various research elaborating stability and reliability issues on GaN HEMTs have been already reported [118–127], albeit few on β-Ga_2O_3 transistors. The earlier efforts in understanding of critical failure mechanisms, their quantification and mitigation have given good returns in terms of improved device performance and possible new applications. Device degradation mainly arises due to the presence of traps in different regions of the device [127], while in high voltage GaN technology it occurs due to the design of epitaxial layer, device layout and topology, and passivation schemes [122]. From the perspective of device characteristics, it is also important to distinguish between temporary and permanent degradation.

7.1. AlGaN/GaN HEMT reliability

Lee et al. [118] reported RF reliability of GaN HEMTs by varying the AlGaN barrier thickness and found reduced barrier thickness of 138 Å improved the output power and efficiency over thicker barrier layer

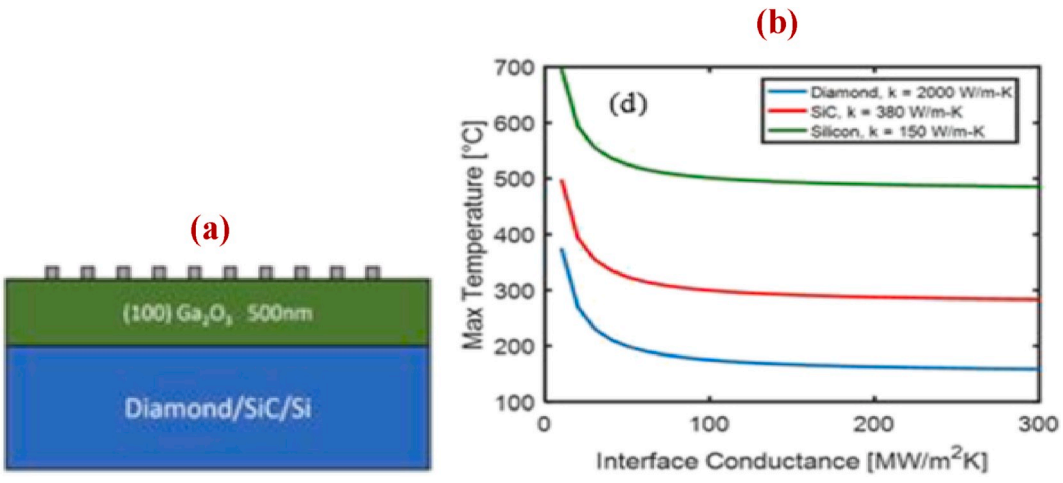

Fig. 14. Thin β-Ga_2O_3 thin membrane integrated on different substrates **(a)** 10 finger device structure with 50 μm gate-to-gate spacing; Ga_2O_3-substrate TBC values were varied from 10 to 300 MWm^{-2} K^{-1} for each substrate material to plot of **(b)** device maximum temperature versus TBC for a diamond, SiC or Si substrate; it was found that TBC was dominant for values less than 70 MW m^{-2} K^{-1} while for lager values thermal conductivity of substrate was more prevailing in device thermal dissipation, figures adapted from Refs. [107].

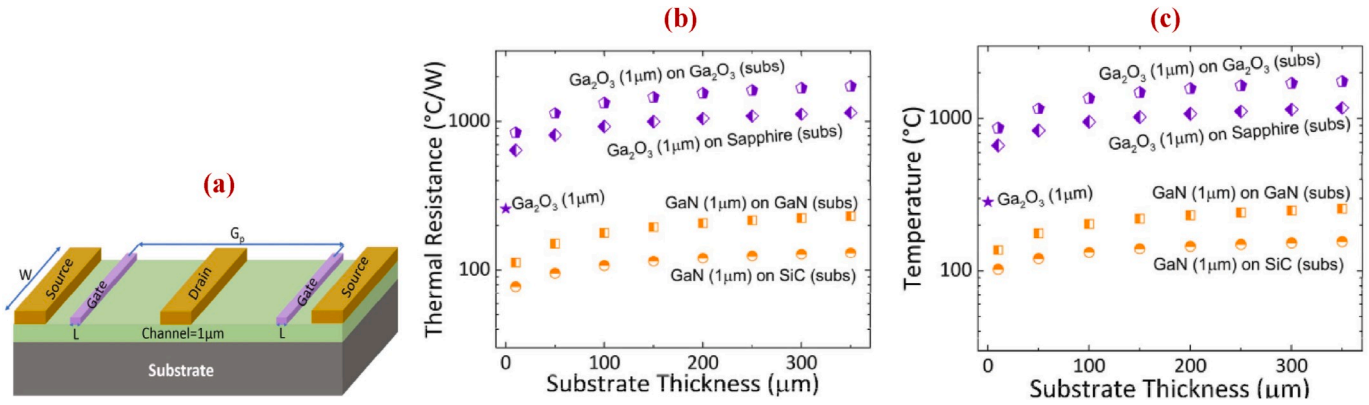

Fig. 15. Estimation of TR and channel temperature of β-Ga_2O_3/GaN HEMTs on different substrates; **(a)** Device schematic with 1 μm channel thickness and gate pitch of 50 μm, **(b)** estimated values of TR (log scale) versus substrate thickness; SiC having k = 3.3 $Wcm^{-1}K^{-1}$ outperform over other substrates in terms of low TR, **(c)** calculated values of channel temperature (log scale) versus substrate thickness; GaN on 350 μm thick SiC showed lowest channel temperature of 160 °C while for Ga_2O_3 on Ga_2O_3 substrate it reached to 1163 °C for even relatively thinner substrate (50 μm). Output power of 10 Wmm^{-1} was assumed and violet color data points as stars are related to device without any substrate in both **(b)** and **(c)**, figures adapted from Ref. [32]. (For interpretation of the references to color in this figure legend, the reader is referred to the Web version of this article.)

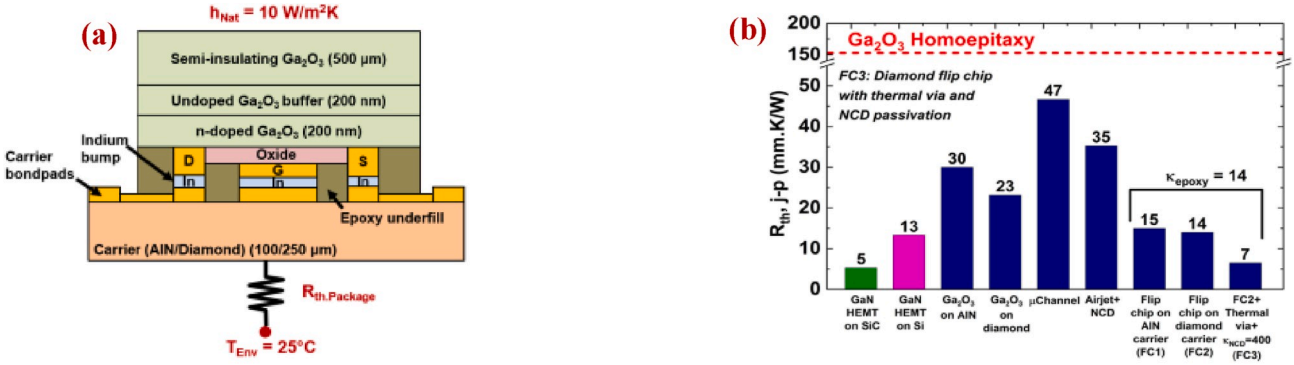

Fig. 16. Top-side cooling technique: Flip-chip hetero-integration of β-Ga_2O_3 onto highly conductive AlN/diamond carrier wafer, **(a)** Device cross-sectional schematic; **(b)** Comparison of thermal performance of different schemes, additional reduction in TR were achieved using NCD passivation and thermal bumps (i.e. heat sinks), comparable values of TRs 13 and 14 mm K W^{-1} are shown for Ga_2O_3 MOSFET and GaN-on-Si HEMT, figures adapted from Refs. [116].

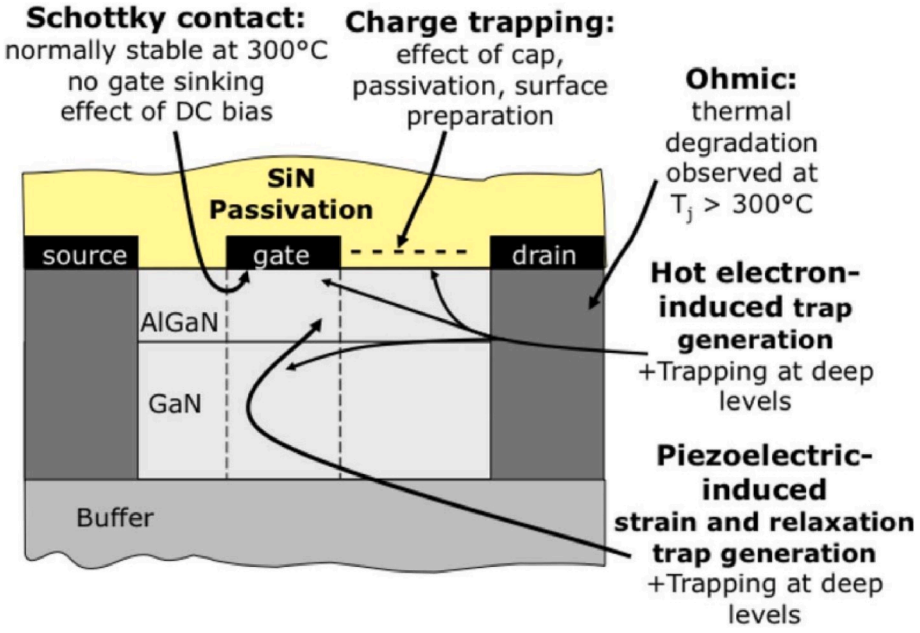

Fig. 17. The schematic of AlGaN/GaN HEMT, highlighting critical areas and associated possible degradation, figure adapted from Ref. [120].

under RF stress of 65 h. Trapping-de-trapping of electrons in surface states was attributed for a discrepancy between DC and RF characteristics [119]. There was no current degradation under DC stress, but under RF exposure for an hour, significant drop in current was observed, although extended RF exposure did not led to further current degradation. This was attributed to deep traps due to shallow impurities and are fully occupied after initial stress [119]. Meneghesso et al. [120] observed parametric and gradual degradation in drain current, transconductance, and more pronounced gate-lag effect in GaN HEMT under both high electric field and channel current. Fig. 17 [120] highlights critical device areas of AlGaN/GaN HEMT prone to distinct failure mechanisms. The initial strain in the AlGaN barrier layer and inverse piezoelectric effect due to high electric field have impacted negatively on device reliability [118,119], which can be mitigated by optimizing initial strain in the barrier and lateral distribution of electric field under the gate [119].

Zanoni et al. [123] reviewed AlGaN/GaN HEMT degradation due to physical effects like inverse piezoelectric effect, stress enabled trap formation and leakage paths, and electrochemical buffer and barrier layer degradation. The authors further suggested various means to improve the reliability of GaN HEMT on SiC/Si. Some of the key recommendations include: lower Al mole fraction in AlGaN barrier layer helps to reduce initial strain and suppressed cracking; a thicker layer of GaN cap (also validated using simulation as shown in Fig. 18 [122]) and/or SiN passivation for delaying surface degradation; optimized SiN deposition; control of hydrogen content and residual strain to minimize surface trapping, current collapse, and hot electron effects.

Khalil et al. [124] demonstrated the operation of life tests to assess the stability and reliability of AlGaN/GaN power HEMTs. The power HEMTs design under test mainly features 3-step field plate arrangements (one gate- and two source-connected filed plates). Room- and High-Temperature Reverse-Bias (RTRB, HTRB), and Operating Life (RTOL, HTOL) measurements were carried out to measure threshold voltage (V_{Th}), on-resistance (R_{ON}), and gate-drain-leakage currents under different stressed time. RTOL tests indicated the positive shift in V_{Th} due to electron trapping in gate stack, degradation of R_{ON} due to reduced gate voltage swing, and a falling trend in gate leakage current versus stress time. HTOL tests show quite different behavior of V_{Th} shift as compared to RTOL, while no impact on R_{ON}—constant value of ~0.7 Ω over entire stress time. Contrary to RTOL, a negative V_{Th} shift was observed during HTOL test and was attributed to electron de-trapping during initial stress time (Region 1). Subsequently, it saturates up to 48 h of stress time (Region 2) due to possible trapping process and followed by a positive shift (Region 3) due to dominant trapping mechanism, and finally saturates (Region 4), all four regions are shown in Fig. 19. A negative shift in V_{Th} is reported under RTRB stress with bias conditions: V_G (−3 V) ‹ V_{Th} and high V_{DS} (200 V) as shown in Fig. 20. A negative shift in V_{Th} is attributed due to detrapping of electrons in the AlGaN barrier layer. This degradation in V_{Th} is fully recoverable with high-temperature annealing albeit partial at room temperature.

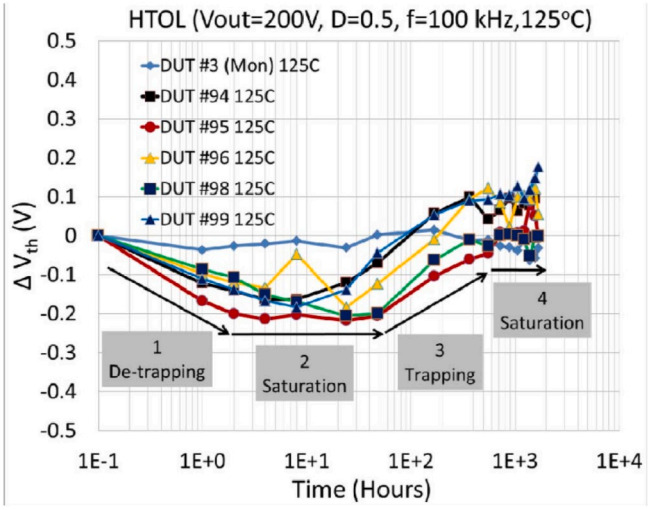

Fig. 19. HTOL tests showing V_{Th} change versus stress time at 125 °C, V_{Th} variation due to trapping/detrapping led positive/negative change followed by saturation region, figure adopted from Ref. [124].

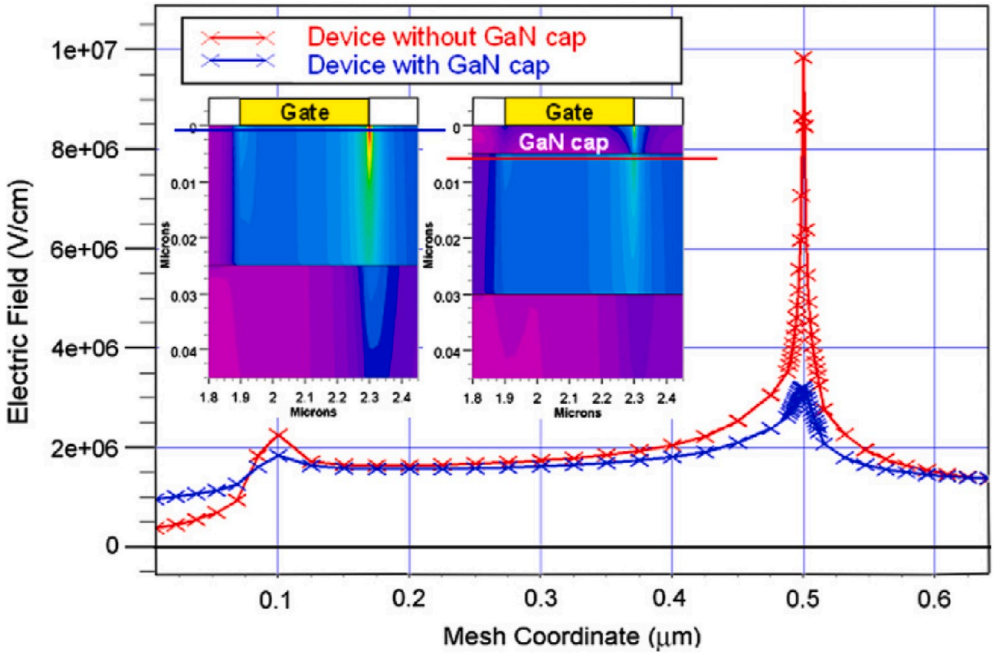

Fig. 18. Simulated electric field profile under the gate of two distinct AlGaN/GaN HEMTs with or without GaN cap, showing 3 × reduced peak electric field in HEMT with GaN cap layer, figure adapted from Ref. [122].

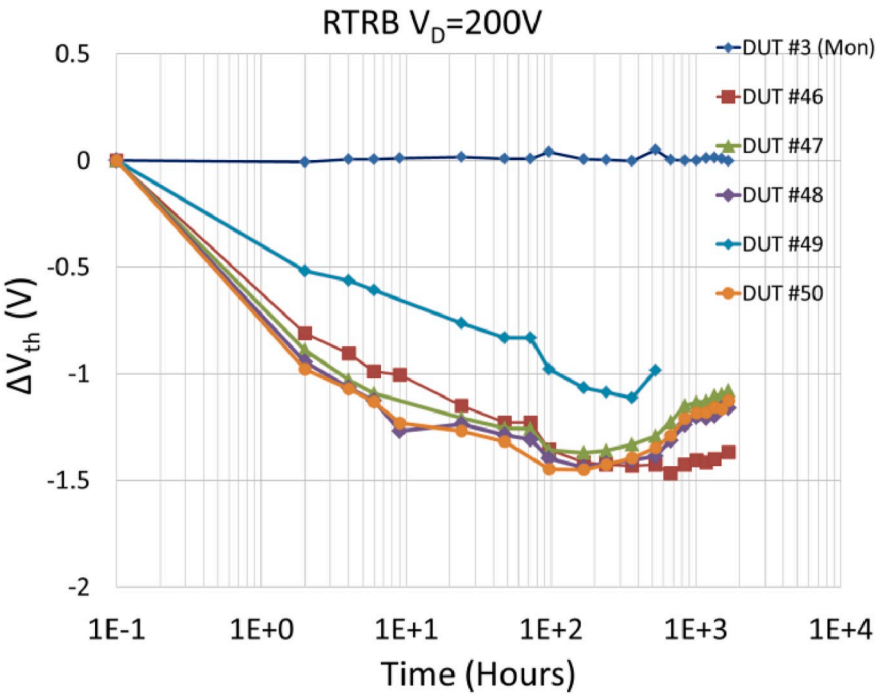

Fig. 20. DC reverse-bias stress test indicating negative V_{Th} shift in range of – 1.1 V to – 1.4 V across all devices under test for long stress time, figure adopted from Ref. [124].

7.2. *β-Ga_2O_3 defects and reliability*

Although there has been significant progress in *β*-Ga_2O_3 based device designs and performance (as discussed in Section 3 and 4), various material defects and related issues are expected to affect device parameters. For an emerging new wide-band gap technology, controlled doping and mitigation of trap-states is critical for device applications [64]. Several experimental studies on defects throughout the entire bandgap of *β*-Ga_2O_3 (010) layers were done using deep level transient spectroscopy (DLTS) and deep level optical spectroscopy (DLOS) techniques [98,128,129]. Various deep level traps, their possible source and key characteristics reported earlier are given in Table 2, out of which two trap levels E_C – 0.7 eV, and E_C – 0.77 eV were identified for V_{Th} instability in *β*-Ga_2O_3 MESFETs [130]. Fe doping in *β*-Ga_2O_3 substrate was attributed as a possible source for these trap levels and total instability of 0.78 V in V_{Th} was estimated for $V_{GS} > V_{Th}$ [130]. Electrons trapping led to reduced channel charge resulted in positive shift of V_{Th}, which is shown in Fig. 21, and the traps filling mechanism at different gate biases using pulsed measurements is shown in Fig. 22. The effect can be mitigated by more optimized growth to reduce trap concentrations near the channel [130].

Looking at the pace of immense research and technological developments of Ga_2O_3 material, there is an exponential rise in related publications on Ga_2O_3 materials and devices. Out of them, some of the important review articles [54,117,131] have left no stone unturned to summarize all related key points with insightful discussion as well as significant value addition at every juncture. Pearton et al. [54] covered properties of Ga_2O_3 material, the role of defects and impurities, recent advances in device fabrication and their performance, as well as current status of WBG based power electronic devices, solar-blind photodetectors, and gas sensors. Recently, Ahmadi et al. [131] reported material issues of α- and β-phases of Ga_2O_3 and their comparison vis-à-vis material properties, growth of bulk-crystal, pros and cons of available device fabrication technology, and resulting device performance. As mentioned by Ahmadi et al. [131], *β*-Ga_2O_3 MODFETs do not help to achieve higher electron mobility (latest reported value is 180 $cm^2 V^{-1}s^{-1}$ at room temperature [73]) due to high electron effective mass and high phonon scattering. In this article we have provided an interesting possibility of AlN/*β*-Ga_2O_3 heterojunction to address the low 2DEG density and small band-offset at the AGO/GO heterojunction. In view of this, this report attempted to include all key aspects of *β*-Ga_2O_3 HEMTs along with regular topics covering properties, and growth of *β*-Ga_2O_3 material, as well as fabrication and performance *β*-Ga_2O_3 devices.

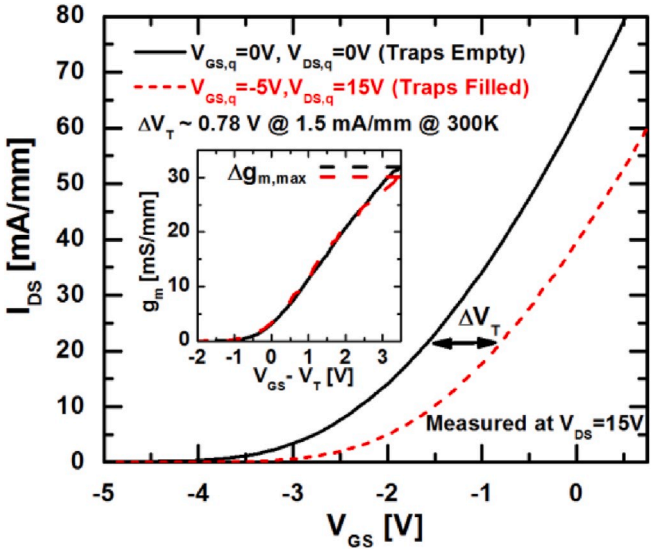

Fig. 21. Transfer characteristics showing V_{Th} dispersion between zero-bias and high V_{DS} quiescent points indicated on graph, Inset: transconductance versus effective gate voltage, figure adapted from Ref. [130].

8. Conclusion

We have attempted to review state-of-the-art technologies of *β*-Ga_2O_3 intended for future power electronic devices. The report

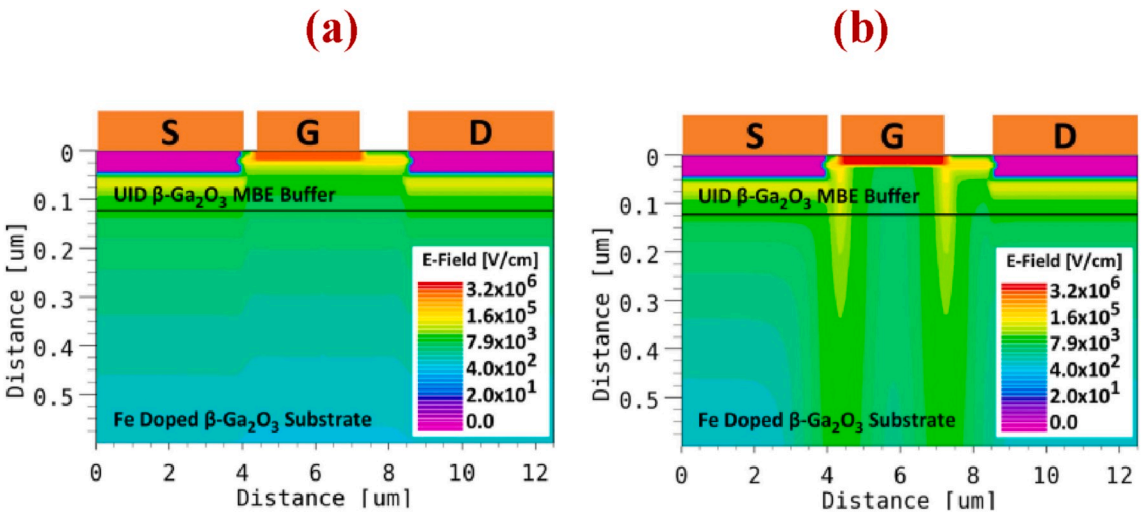

Fig. 22. Simulated electric field profiles **(a)** before and **(b)** after the pinch-off, under effective gate voltage 1.5 V and −1.6 V respectively, beyond pinch-off electric fields extending up to substrate through buffer layer. The high gate leakage current in the high V_{DS}-off condition due to injection of large number of electrons into the device, figures adapted from Refs. [130].

summarized Ga_2O_3 material developments starting from bulk single crystals to high-quality large-size wafers; epitaxial growth techniques—MBE and PA-MBE for device-quality epitaxial wafers to make β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ heterostructure; carrier confinement at the heterointerface for the evolution of first MODFET and finally introduction of Si-delta doping and spacer layer for more controlled dopant concentration and subsidized coulomb scattering respectively. Later part of the report summarized the growth of III-nitrides using MOCVD on β-Ga_2O_3 for the formation of possible AlN/β-Ga_2O_3 heterojunction, and calculation of 2DEG density due to spontaneous and piezoelectric polarization using widely reported polarization constants. Band-offset of β-Ga_2O_3 at the AlN/β-Ga_2O_3 heterojunction and its effects on 2DEG density are discussed amid quest of more confined higher 2DEG density. Self-heating effects in β-Ga_2O_3 devices due to its low thermal conductivity and so inevitable device thermal management are discussed. Reliability and failure mechanisms of WBG based devices due to various defects and design topologies are also discussed along with their effective mitigation.

Being the least mature technology among WBG semiconductors, β-Ga_2O_3 has achieved significant signs of progress: Schottky diodes on Sapphire with breakdown voltage >2 kV, E− and D-mode MOSFETs with critical fields ~5 $MVcm^{-1}$ which is twice of GaN or SiC values. Furthermore, β-Ga_2O_3 FETs have shown record high drain current density of ~1.5 A mm^{-1} and are comparable to GaN FETs, although the RF performance of β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ HFETs are lagging behind their GaN counterparts. For β-Ga_2O_3 devices in order to contribute a significant role in high frequency and high power applications, rigorous and sustained research is highly essential for a breakthrough. In order to achieve excellent device performance of β-Ga_2O_3 in power electronic applications, there are several key bottleneck areas where further research will produce huge benefits. Some of them are surface morphology of doped β-Ga_2O_3 thin films, development of high quality bulk crystals with minimum defects, growth of high quality homo- and hetero-epitaxial layer with controlled doping on β-Ga_2O_3 substrates, sustainable thermal management approaches for high power devices, as well as more research to explore opportunities of p-type doping in β-Ga_2O_3.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Appendix A. Supplementary data

Supplementary data to this article can be found online at https://doi.org/10.1016/j.mssp.2020.105216.

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